IN THE CLAIMS

Please amend the claims as indicated below.

1. (currently amended) A wafer-level chip scale package, comprising:

a chip containing a stud bump;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate.

2. (original) The package of claim 1, wherein at least one conductive particle is located between the stud bump and the bond pad.

3. (original) The package of claim 1, wherein the conductive particles comprise metal with an insulating layer.

4. (original) The package of claim 1, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

5. (original) The package of claim 1, wherein the chip contains an integrated circuit in communication with a chip pad.

6. (previously presented) The package of claim 1, wherein the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

7. (previously presented) The package of claim 1, wherein the package does not contain any solder paste.

8. (original) The package of claim 1, wherein the stud bump comprises Cu.

9. (original) The package of claim 8, wherein the stud bump is a coined stud bump.

10. (original) The package of claim 1, wherein the chip does not contain a chip pad overlying an integrated circuit.

11. (currently amended) A wafer-level chip scale package, comprising:

a chip containing a stud bump comprising Cu;

a substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate with at least one conductive particle contacting both the stud bump and the bond pad, wherein the conductive particles comprise a metal with an insulating layer.

12. (original) The package of claim 11, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

13. (previously presented) The package of claim 11, wherein the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern

14. (previously presented) The package of claim 11, wherein the package does not contain any solder paste.

15. (currently amended) A packaged semiconductor device, comprising:

a chip containing a stud bump comprising Cu;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate with at least one conductive particle contacting both the stud bump and the bond pad, wherein the conductive particles comprise a metal with an insulating layer.

16. (original) The device of claim 15, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

17. (previously presented) The device of claim 15, wherein the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

18. (previously presented) The package of claim 15, wherein the device does not contain any solder paste.

19. (currently amended) An electronic apparatus containing a packaged semiconductor device without solder paste, the device comprising:

a chip containing a stud bump;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles contacting both the chip and the substrate, wherein the conductive particles comprise a metal with an insulating layer.

20. (canceled)

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27. (canceled)

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30. (canceled)

31. (canceled)

32. (canceled)

33. (currently amended) A wafer-level chip scale packaged semiconductor device, the device comprising:

a chip containing a stud bump;

a substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate, wherein the conductive particles comprise a metal with an insulating layer.

34. (previously presented) The device of claim 33, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

35. (previously presented) The device of claim 35, wherein the chip contains a re-distributed line (RDL) pattern underlying the stud bump with an insulating layer covering a portion of the RDL pattern.

36. (previously presented) The device of claim 33, wherein the packaged device does not contain solder paste.

37. (currently amended) An electronic apparatus containing a wafer-level chip scale packaged semiconductor device, the device comprising:

a chip containing a stud bump;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate.

38. (previously presented) The device of claim 37, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

39. (previously presented) The device of claim 37, wherein the chip contains a re-distributed line (RDL) pattern underlying the stud bump with an insulating layer covering a portion of the RDL pattern.

40. (previously presented) The device of claim 37, wherein the packaged device does not contain solder paste.

41. (currently amended) A wafer-level chip scale package without solder paste, comprising:

a chip containing a stud bump;

a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate, wherein a conductive particle contacts both the stud bump and the bond pad, wherein the conductive particles comprising a metal with an insulating layer.

42. (previously presented) The package of claim 41, wherein the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

43. (previously presented) The package of claim 41, wherein the chip contains a re-distributed line (RDL) pattern underlying the stud bump with an insulating layer covering a portion of the RDL pattern.

44. (previously presented) The package of claim 41, wherein the stud bump comprises Cu.

45. (previously presented) The package of claim 41, wherein the stud bump is a coined stud bump.